DEC Chip Design Contest

A Fully Integrated Switched-Capacitor Voltage Regulator With Dynamic Body Biasing on Power Switches for Energy-Efficient DNN Accelerators

Seokwon Jung, Junseo An, Seungchae Lim and Jun-Eun Park Department of Electrical and Computer Engineering Sungkyunkwan University, Suwon, Republic of Korea

Abstract

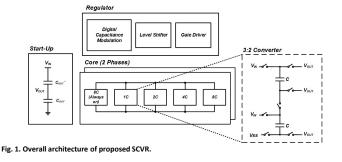
A fully integrated on-chip switched capacitor voltage regulator (SCVR) with a 3:2 conversion ratio and digital capacitance modulation (DCM) is used for efficient power delivery. The proposed dynamic body biasing (DBB) improves power efficiency, achieving a peak of 89% at 30 mA and providing a 2–3% improvement under heavy loads. The regulator demonstrates a 70mV voltage droop and 130ns settling time for a 50ns current step.

Proposed Design

• The proposed SCVR uses a 3:2 switched capacitor DC-DC converter with digital capacitance modulation (DCM) for dynamic capacitor adjustment based on load variations.

• **Dynamic body biasing (DBB)** is applied to the power switches, improving efficiency by reducing on-resistance under heavy load conditions.

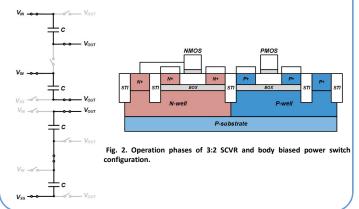
• **On-chip MIM capacitors** are utilized to achieve high power density, while a stack capacitor supports auxiliary power rail generation during startup.



Dynamic Body Biasing

• **Dynamic body biasing (DBB)** is implemented to optimize the power efficiency of the SCVR by reducing the on-resistance of power switches under heavy load conditions.

• **DBB applies** forward body bias when the switch is on, minimizing on-resistance, and removes the bias when the switch is off to prevent leakage current.

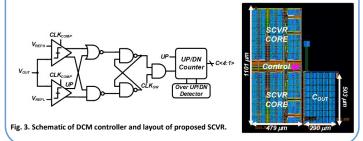


Digital Capacitance Modulation

• **Digital capacitance modulation (DCM)** dynamically adjusts the number of capacitors in the SCVR based on variations in the load current, optimizing voltage regulation.

• **DCM detects voltage changes** caused by load fluctuations and activates or deactivates capacitors to maintain a stable output voltage.

• This method enables a fixed switching frequency for the SCVR, making it easier to achieve regulation in the following linear regulator and simplifying EMI-related analysis.



Simulations Results

• The proposed SCVR achieves a peak efficiency of 89% at 30mA, with a 2–3% improvement in power efficiency under heavy load conditions using DBB.

• Transient simulations show a voltage droop of 70mV and a settling time of 130ns for a 50ns current step, demonstrating fast response and stable performance.

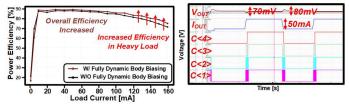


Fig. 4. Simulated power efficiency versus load current, and load transient response of SCVR.

Conclusions

The proposed on-chip SCVR with DCM and FDBB achieves high power efficiency and stable voltage regulation. Simulation results show a peak efficiency of 89% and improved performance under heavy loads. The design demonstrates fast transient response with minimal voltage droop, making it suitable for power-sensitive applications.

Reference

T. Souvignet, B. Allard and S. Trochut, "A Fully Integrated Switched-Capacitor Regulator With Frequency Modulation Control in 28-nm FDSOI," in IEEE Transactions on Power Electronics, vol. 31, no. 7, pp. 4984-4994, July 2016.

